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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,509	07/30/2001	Katsuhiko Hieda	04329.2613	8843

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Finnegan, Henderson, Farabow
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER	
LE, THAO X	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,509	HIEDA, KATSUHIKO	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *3-21 and 24-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,22,23 and 35-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species 1, Figs. 1-11B, claims 1, 2, 22, 23, and 35-43 in Paper No. 6 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. '...the source and the drain region changes on the side surface of the convex semiconductor layer' in claim 1 is not clear.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1, 2, 22, 23, 35-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,567,962 to Miyawaki et al.

Regarding to claim 1, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1013/1016/1021, fig 17, provided on a semiconductor substrate, a source region 1030, column 10 line ~~23~~ 32, and a drain region 1017 column 9 line 59 in the convex semiconductor layer, and a gate electrode 1023, column 10 line 11 having side-wall gate portion 1023, fig. 12, and column 6 line 53-61, provided over ~~a side~~ a side surface of the convex semiconductor layer, wherein the distance between the source (S) region and drain (D) region changes on the side surface of the convex semiconductor layer, fig. 25 where the channel 1021 is not uniform. But, Miyawaki does not expressly disclose in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the S/D regions, via at least the side surface of the convex semiconductor layer. However, it would have been obvious to one of ordinary skill in the art to applying the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known the art.

Regarding to claim 2, Miyawaki discloses a semiconductor device comprising a convex semiconductor layer 1013/1016/1021, fig 17, provided on a semiconductor substrate, a source region 1030, column 10 line 23, and a drain region 1017 column 9 line 59 in the convex semiconductor layer, and a gate electrode 1023, column 10 line 11 having side-wall gate portion 1023, fig. 12, and column 6 line 53-61, provided over a side a side surface of the convex semiconductor layer, and the side-wall insulating film 1022, fig. 12 column 10 line 9, on a side surface of the gate electrode and the side surface of the convex semiconductor layer. But, Miyawaki does not expressly disclose in an

insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the S/D regions, via at least the side surface of the convex semiconductor layer. However, it would have been obvious to one of ordinary skill in the art to applying the voltage to the gate electrode to create the electric field effect to a channel region, because such transistor function is well known the art.

Regarding to claim 22, Miyawaki discloses a semiconductor device wherein the side-wall gate portion is offset with respect to a part of the source region and the drain region, fig. 25

Regarding to claim 23, Miyawaki discloses a semiconductor device wherein the semiconductor region P, having a impurity concentration higher than that of the channel region P-, column 13 line 9-12, the semiconductor region provided between the substrate and the S/D region and between the substrate and the channel region, fig. 25.

Regarding to claim 35, Miyawaki discloses a semiconductor device wherein a distance between the S/D regions becomes longer toward a lower portion from the upper portion of the convex semiconductor layer.

Regarding to claim 36, Miyawaki discloses a semiconductor device wherein the impurity concentration of the S/D region becomes lower toward a lower portion from an upper portion of the convex semiconductor layer, column 15 line 26. This is also known as LDD structure

Regarding to claim 37, Miyawaki discloses a semiconductor device wherein the side-wall gate portion is formed to portion under the S/D region along the side surface of the convex semiconductor layer, fig. 10, 11, 12, and 13.

Regarding to claim 38, Miyawaki does not disclose a semiconductor device wherein a width of the convex semiconductor layer is smaller than 0.2 μm. But Miyawaki discloses the width d_3 of the channel, column 6 line 63 and column13 line 49-51. This width would be corresponding to the width of the convex semiconductor layer.

Regarding to claim 39, Miyawaki discloses a semiconductor device wherein a width of the convex semiconductor layer is smaller than the depth of the S/D region. The depth of S/D regions 1030/1017, fig. 11-14, would be corresponding to d_1 and $d_3<d_1$, column 10 line 55.

Regarding to claim 40, 41, 42, Miyawaki discloses a semiconductor device wherein at least one of the S/D regions includes at least two kinds of diffusion layers 1030 and 1085, a high and low concentration N^+ and N^-, having a dense impurity concentration diffusion layer, and the convex semiconductor is electrically connected to the conductive substrate, fig 25

Regarding to claim 43, Miyawaki discloses a semiconductor device comprising a gate insulating film 1022 is made of a Si oxide, column 10, line 9.

Regarding to claim 44, 45, Miyawaki discloses a semiconductor device wherein a position of a deepest portion of the gate electrode is deeper that a position of the deepest portion of the S/D region, fig. 10, 11, 12, and 13.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
May 9, 2002

PHAT X. CAO
PRIMARY EXAMINER